circuit can be prevented.

Figs. 17A to 17J are cross-sectional views showing fabrication steps of the semiconductor apparatus, shown in Fig. 13. Each of Figs. 17A to 17F shows only a part of wafer. In fabrication, first, a wafer 20, on which a plurality of semiconductor device 11 is formed, is provided.

Next, as shown in Fig. 17A, electrode pads 12 and an oxide layer 25 are formed on a substrate. Then grooves 26 are formed on dicing lines of the wafer 20 to have a depth of 100 to 200 $\mu$m.

In a process shown in Fig. 17B, an insulating layer 27 is formed on the wafer 20 so that the grooves 26 are filled with the insulating layer 27 but a part of the electrode pad 12 of the semiconductor devices is not covered with the insulating layer 27. The insulating layer 27 may be of polyimide resin. The insulating layer 27 formed on the oxide layer 25 to have a thickness of several $\mu$m is later functioning as the insulating layer 23, shown in Fig. 14. On the other hand, the insulating layer 27 filled in the grooves 26 is later functioning as the insulating 27, shown in Fig. 14.

Next, as shown in Fig. 17C, a metal layer 28 is formed over the wafer 20. In other words, the insulating layer 27 and the exposed electrode pads 12 are covered with the metal layer 28. Subsequently, as shown in Fig. 17D, a rewiring layer 13 is formed on selective areas of the metal layer 28. The selective areas are used for electrical connection.

Referring to Fig. 17E, a conductive post material 14 is formed on the rewiring layer 13 to extend across the groove 26. The post material 14 is used for two individual conductive posts after the wafer 20 is diced into individual semiconductor apparatuses. Next, as shown in Fig. 17F, unnecessary parts of the metal layer 28 is removed. As shown in Fig. 17G, after that, the semiconductor wafer 20 is molded with a molding resin 15 so that an upper surface of the molding resin 15 is on the same plane with upper surfaces of the conductive post material 14.

Subsequently, as shown in Fig. 17H, the molding resin 15 is polished with a polishing device 21 until the post material 14 is exposed. Next, as shown in Fig. 17I, solder balls (conductive bumps) 16 are formed on upper ends of the conductive posts 14. Then, as shown in Fig. 17J, the semiconductor wafer 20 is diced along the dicing lines 19 to form a plurality of individual semiconductor apparatus using a cutter blade 22.

As described above, according to the third preferred embodiment of the present invention, the insulating layer 27 is filled in the grooves so that the insulating layer 23 is formed on the semiconductor devices 11 and at the same time the insulating layer 24 is formed on the peripheral side surface of the semiconductor devices 11 entirely.

Fourth Preferred Embodiment

Fig. 18 is a cross-sectional view showing a part of a semiconductor apparatus according to a fourth preferred embodiment of the present invention. Fig. 19 is a cross-sectional view showing an enlarged part of the semiconductor apparatus, shown in Fig. 18. In this embodiment, the same or corresponding elements to those in the above described embodiments are represented by the same reference numerals.

The semiconductor apparatus includes a semiconductor device (element) 11; a plurality of electrode pads 12; a rewiring pattern 13; a plurality of conductive posts 14, connected through the rewiring pattern 13 to the electrode pads 13; a mold resin 15 shaped to have an upper surface on the same plane with upper surfaces of the conductive posts; solder balls 16 provided on upper ends of the conductive posts14; and solder bumps 29 provided on side surfaces of the conductive posts 14.

The electrode pads 12 are connecting electrodes, made of aluminum (Al), for the semiconductor devices 11. The rewiring pattern 13, connecting the electrode pads 12 and the posts 14, is made of copper (Cu). The posts 14 are made of copper (Cu) to be pillar shape. The molding resin 15 is shaped to have a peripheral side surface that is on the identical plane with a peripheral side surface of the semiconductor device 11.

According to the fourth preferred embodiment, the solder

bumps 29 are provide on the side surfaces of the conductive posts 14, so that a better solderbility or wetting condition can be obtained when the semiconductor apparatus is mounted on a circuit board. As a result, mechanical strength of soldered portions is improved. Further in the same manner as the third preferred embodiment, occurrence of short circuit is well prevented.

Namely, according to the fourth preferred embodiment, the solder bumps 29 are provide on the side surfaces of the conductive posts 14, so that mechanical strength of soldered portions is improved as compared to the third preferred embodiment.

Figs. 20A to 20C are cross-sectional views showing fabrication steps of the semiconductor apparatus, shown in Fig. 18. Semiconductor apparatuses, shown in Fig. 20A, are formed by dicing the semiconductor wafer 20, shown in Fig. 17J. That is, Fig. 20A follows Fig. 17J.

Now referring to Fig. 20B, the distance between two adjacent semiconductor apparatus (devices) 11 are expanded. Since individual semiconductor apparatus are usually mounted on a tape, the tape is expanded to widen the distance between two adjacent semiconductor apparatus (devices) 11. Next, as shown in Fig. 20C, thus distanced semiconductor devices are reflowed, for example at 230℃. As a result, the solder balls 16 on the posts 14 are melted and a solder bump 29 is formed on a peripheral side surface of each of the conductive posts 14.